REMARKS

Applicant has carefully reviewed and considered the Office Action mailed on November 20, 2002, and the references cited therewith. Claims 4 and 14 are amended. Claims 4-6, 9-10 and 14-16 are now pending in this application. Applicant does not admit that the cited references are prior art and reserves the right to "swear behind" each of the cited references as provided under 37 C.F.R. 1.131.

§102 Rejection of the Claims

Claims 4, 14, and 15 were rejected under 35 USC § 102(e) as being anticipated by Manning et al. (U.S. Patent No. 5,962,887).

With regard to claim 4, among the differences, claim 4, as amended, recites "the transistor to operate in the depletion mode wherein the transistor is to remove charge at a constant rate for a non-linear voltage variation." (emphasis added). The Office Action indicated that claim 4 was anticipated by Figures 1 and 2 and accompanying description at column 1, line 59 – column 2, line 19 in Manning. Applicant respectfully submits that these citations in Manning do not teach an operation of the transistor in the depletion mode wherein the transistor is to remove charge at a constant rate for a non-linear voltage variation. In contrast, Manning discloses the operation of a transistor above the threshold voltage, Vt, and specifically teaches away from operation below the threshold voltage because a "reduced capacitance" below the threshold voltage See Manning at column 2, lines 14-18. In particular, Figure 2 illustrates the associated capacitance voltage curve for Figure 1, wherein the operation of the transistor is in a range beyond the threshold voltage wherein the voltage is linear. Therefore, the operation of the transistor of Figure 1 is such that the operating voltage for the transistor is linear. Accordingly, Applicant respectfully submits that the rejection of claim 4 has been overcome and that this claim is in condition for allowance.

With regard to claim 14, among the differences, claim 14, as amended, recites "an electronic device having a variable capacitance characteristic and that is permanently coupled between the ground node and the power supply voltage node and capable of providing a removal of charge at a constant rate for an asymmetrical incremental voltage variations about an operational node voltage at the power supply voltage node. (emphasis added). The Office Action indicated that claim 14 was anticipated by Figures 1 and 2 and accompanying description

at column 1, line 59 – column 2, line 19 in Manning. Applicant respectfully submits that these citations in Manning do not teach an operation of an electronic device having a variable capacitance characteristic wherein the removal of charge at a constant rate for an asymmetrical incremental voltage variations. As set forth above, in contrast, Manning discloses the operation of a transistor above the threshold voltage, Vt, and specifically teaches away from operation below the threshold voltage because a "reduced capacitance" below the threshold voltage See Manning at column 2, lines 14-18. In particular, Figure 2 illustrates the associated capacitance voltage curve for Figure 1, wherein the operation of the transistor is in a range beyond the threshold voltage wherein the voltage is linear. Therefore, the operation of the transistor of Figure 1 is such that the operating voltage for the transistor is linear. Accordingly, Applicant respectfully submits that the rejection of claim 14 has been overcome and that this claim is in condition for allowance.

Claims 9 and 10 were rejected under 35 U.S.C. § 102(b) as being anticipated by Mead et al. (U.S. Patent No. 5,844,265). Applicant respectfully traverses this rejection. Among the differences, claim 9 recites "a transistor coupled between the high power supply voltage node and the low power supply voltage node and operable for controlling a voltage at the low power supply voltage node." (emphasis added). The Office Action indicated that this limitation was disclosed by Figure 1 in Mead. In particular, the Office Action equated element 32, input line 18 and output node 28 of Figure 1 to the transistor, the high power supply voltage node and the low power supply voltage node in claim 9, respectively. Applicant respectfully traverses this assertion. The circuit illustrated in Figure 1 of Mead is a "sense amplifier". See Mead at column 2, lines 61-65. Mead does not disclose that the output node 28 is or is coupled to a low power voltage. Moreover, Mead does not disclose that the element 32 is "operable for controlling a voltage at the low supply voltage node" because such element is not coupled to a low power supply voltage node.

Accordingly, Applicant respectfully submits that the rejection of claim 9 has been overcome and that this claim is in condition for allowance. Because claim 10 depends from and further defines claim 9, Applicant respectfully submits that the rejection of claim 10 has been overcome and that this claim is in condition for allowance.

§103 Rejection of the Claims

Claims 5, 6, and 16 were rejected under 35 USC § 103(a) as being unpatentable over Manning et al. (U.S. Patent No. 5,962,887). Because claims 5, 6 and 16 depend from and further define claims 4 and 14, respectively, Applicant respectfully submits that the rejections of claims 5, 6 and 16 have been overcome and that these claims are in condition for allowance.

Interview Summary

Applicant's representative (Gregg A. Peacock) and Examiner Quan Tra met March 19, 2003 to discuss the differences in the cited art and the pending claims.

Conclusion

Applicant respectfully submits that the claims are in condition for allowance and notification to that effect is earnestly requested. The Examiner is invited to telephone Applicant's attorney ((612) 371-2103) to facilitate prosecution of this application.

If necessary, please charge any additional fees or credit overpayment to Deposit Account No. 19-0743.

Respectfully submitted,

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Date March 20, 2003 By _____
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CERTIFICATE UNDER 37 CFR 1.8: The undersigned hereby certifies that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail, in an envelope addressed to: Commissioner of Patents, Washington, D.C. 20231, on this 20th day of March, 2003.

Anne M. Richards _____

Name Signature